This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 (previously presented): A semiconductor integrated circuit device comprising:

a semiconductor substrate on which a plurality of transistors ~~including~~ having gate insulation films of three or more different thicknesses are formed; and

an input/output terminal formed on the semiconductor substrate, wherein a transistor physically connected directly to the input/output terminal is one of the transistors other than a transistor having the thinnest gate insulation film.

2 (previously presented): A semiconductor integrated circuit device according to claim 1, further comprising a power supply terminal to which an external power supply voltage is applied, wherein a transistor connected directly to the power supply terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

3 (previously presented): A semiconductor integrated circuit device according to claim 1, further comprising a power supply terminal to which an external power supply voltage is applied and a ground terminal, wherein a transistor having a current path connected between the power supply terminal and the ground terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

4 (previously presented): A semiconductor integrated circuit device according to claim 1, further comprising an interface circuit connected to the input/output terminal, wherein a transistor included in the interface circuit and connected directly to the input/output terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

5 (previously presented): A semiconductor integrated circuit device according to claim 4, wherein a transistor included in the interface circuit and connected directly to a power supply terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

6 (previously presented): A semiconductor integrated circuit device according to claim 5, wherein a transistor included in the interface circuit and having a current path connected between the power supply terminal and a ground terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

7 (original): A semiconductor integrated circuit device according to claim 4, wherein said interface circuit includes an input buffer circuit.

8 (original): A semiconductor integrated circuit device according to claim 4, wherein said interface circuit includes an output buffer circuit.

9 (original): A semiconductor integrated circuit device according to claim 4, wherein said interface circuit includes a level shifter and an output buffer circuit.

10 (withdrawn): A semiconductor integrated circuit device according to claim 1, further comprising a regulator circuit, a transistor which constitutes part of the regulator circuit and is connected directly to the power supply terminal being one of the transistors other than the transistor having the thinnest gate insulation film.

11 (withdrawn): A semiconductor integrated circuit device according to claim 10, wherein a transistor which constitutes part of the regulator circuit having a current path connected between the power supply terminal and a ground terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

12 (withdrawn): A semiconductor integrated circuit device according to claim 1, further comprising a regulator circuit, a transistor which is connected directly to an output node of the regulator circuit is the transistor having the thinnest gate insulation film.

13 (original): A semiconductor integrated circuit device according to claim 9, further comprising a regulator circuit, said level shifter converting a lowered potential level signal obtained from the regulator circuit into a power supply voltage level signal to be supplied to an external terminal.

14 (previously presented): A semiconductor integrated circuit device according to claim 13, wherein a transistor included in the level shifter and a device directly receiving the lowered potential level signal is the transistor having the thinnest gate insulation film.

15 (withdrawn): A semiconductor integrated circuit device according to claim 1, further comprising a sensing circuit, connected to the input/output terminal, for sensing a third high level voltage input which is higher than an external power supply voltage, a transistor which constitutes part of the sensing circuit and is connected directly to the input/output terminal being one of the transistors other than the transistor having the thinnest gate insulation film.

16 (withdrawn): A semiconductor integrated circuit device according to claim 15, wherein a transistor which constitutes part of the sensing circuit and is connected directly to a power supply terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

17 (withdrawn): A flash EEPROM (electrically erasable programmable read-only memory) comprising:

a memory cell array formed on a semiconductor substrate; and

a control circuit, formed on the semiconductor substrate and connected to a plurality of memory cells that constitute the memory cell array, for controlling nodes of the memory cells, said control circuit including a Y-selector whose gate is applied with an internally boosted voltage at a time of reading.

18 (withdrawn): A flash EEPROM according to claim 17, wherein a plurality of transistors including gate insulation films of different thicknesses are formed on the semiconductor substrate, and said Y-selector is formed of a transistor which is other than a transistor having the thinnest gate insulation film.

19 (withdrawn): A flash EEPROM (electrically erasable programmable read-only memory) comprising:

a memory cell array formed on a semiconductor substrate; and

a control circuit, formed on the semiconductor substrate and connected to a plurality of memory cells that constitute the memory cell array, for controlling nodes of the memory cells, said control circuit including a source decoder whose NMOS driver gate is applied with an internally boosted voltage at a time of reading.

20 (withdrawn): A flash EEPROM according to claim 19, wherein a plurality of transistors including ate insulation films of different thicknesses are formed on the semiconductor substrate, and said source decoder is formed of a transistor which is other than a transistor having the thinnest gate insulation film.

21 (currently amended): A semiconductor integrated circuit device comprising:

a semiconductor substrate on which a plurality of transistors ~~including~~ having gate insulation films of three or more different thicknesses are formed; and

an input/output terminal formed on the semiconductor substrate, wherein a transistor connected directly to the input/output terminal, absent any intervening elements, is one of the transistors other than a transistor having the thinnest gate insulation film.

22 (previously presented): A semiconductor integrated circuit device according to claim 21, further comprising a power supply terminal to which an external power supply voltage is applied, wherein a transistor connected directly to the power supply terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

23 (previously presented): A semiconductor integrated circuit device according to claim 21, further comprising a power supply terminal to which an external power supply voltage is applied and a ground terminal, wherein a transistor having a current path connected between the power supply terminal and the ground terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

24 (previously presented): A semiconductor integrated circuit device according to claim 21, further comprising an interface circuit connected to the input/output terminal, wherein a transistor included in the interface circuit and connected directly to the input/output terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

25 (previously presented): A semiconductor integrated circuit device according to claim 24, wherein a transistor included in the interface circuit and connected directly to a power supply terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

26 (previously presented): A semiconductor integrated circuit device according to claim 25, wherein a transistor included in the interface circuit and having a current path connected between the power supply terminal and a ground terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

27 (previously presented): A semiconductor integrated circuit device according to claim 24, wherein said interface circuit includes an input buffer circuit.

28 (previously presented): A semiconductor integrated circuit device according to claim 24, wherein said interface circuit includes an output buffer circuit.

29 (previously presented): A semiconductor integrated circuit device according to claim 24, wherein said interface circuit includes a level shifter and an output buffer circuit.

30 (previously presented): A semiconductor integrated circuit device according to claim 29, further comprising a regulator circuit, said level shifter converting a lowered potential level signal obtained from the regulator circuit into a power supply voltage level signal to be supplied to an external terminal.

31 (previously presented): A semiconductor integrated circuit device according to claim 30, wherein a transistor included in the level shifter and a device directly receiving the lowered potential level signal is the transistor having the thinnest gate insulation film.

32 (currently amended): A semiconductor integrated circuit device comprising:

a semiconductor substrate on which a plurality of transistors ~~including~~ having gate insulation films of three or more different thicknesses are formed; and

an input/output terminal formed on the semiconductor substrate, wherein a transistor always connected directly to the input/output terminal is one of the transistors other than a transistor having the thinnest gate insulation film.

33 (previously presented): A semiconductor integrated circuit device according to claim 32, further comprising a power supply terminal to which an external power supply voltage is applied, wherein a transistor connected directly to the power supply terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

34 (previously presented): A semiconductor integrated circuit device according to claim 32, further comprising a power supply terminal to which an external power supply voltage is applied and a ground terminal, wherein a transistor having a current path connected between the power supply terminal and the ground terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

35 (previously presented): A semiconductor integrated circuit device according to claim 32, further comprising an interface circuit connected to the input/output terminal, wherein a transistor included in the interface circuit and connected directly to the input/output terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

36 (previously presented): A semiconductor integrated circuit device according to claim 35, wherein a transistor included in the interface circuit and connected directly to a power supply terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

37 (previously presented): A semiconductor integrated circuit device according to claim 36, wherein a transistor included in the interface circuit and having a current path connected between the power supply terminal and a ground terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

38 (previously presented): A semiconductor integrated circuit device according to claim 35, wherein said interface circuit includes an input buffer circuit.

39 (previously presented): A semiconductor integrated circuit device according to claim 35, wherein said interface circuit includes an output buffer circuit.

40 (previously presented): A semiconductor integrated circuit device according to claim 35, wherein said interface circuit includes a level shifter and an output buffer circuit.

41 (previously presented): A semiconductor integrated circuit device according to claim 40, further comprising a regulator circuit, said level shifter converting a lowered potential level signal obtained from the regulator circuit into a power supply voltage level signal to be supplied to an external terminal.

42 (previously presented): A semiconductor integrated circuit device according to claim 41, wherein a transistor included in the level shifter and a device directly receiving the lowered potential level signal is the transistor having the thinnest gate insulation film.